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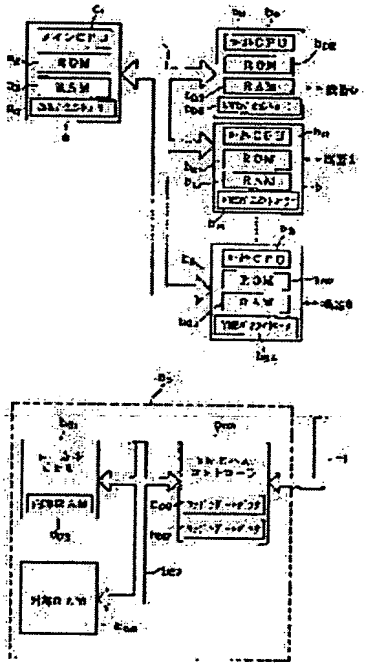
(54) INDUSTRIAL COMPUTER

(57)Abstract:
PURPOSE: To provide an industrial computer which effectively uses the internal memory of an IC for CPU.
CONSTITUTION: An input/output board b0, which is provided with an internal RAM b05 and an external RAM b06 storing their own operation information and a VME bus controller b04 and is controlled based on control data inputted to the VME bus controller b04 through a VME bus 1, and a main CPU board (a) which is provided with a VME bus controller a4 communicating with the VME bus controller b04 and reads out operation information stored in the internal RAM b05 and the external RAM b06 to monitor and control the operation of the input/output board b0 are provided, and mapping registers b08 and b09 which assign the addresses of the internal RAM b05 and the external RAM b06 to the address space of the VME bus 1 are provided in the VME bus controller b04 correspondingly to the internal RAM b05 and the external RAM b06.



LEGAL STATUS

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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The I / O board controlled based on the control data which has two or more storage means and 1st means of communications which memorize their performance information, and is inputted into this means of communications through a system bus, It has said 1st means of communications and the 2nd means of communications which communicates through said system bus. In the industrial computer possessing the main board which reads the performance information memorized by said storage means, and supervises and controls actuation of said I / O board by this 2nd means of communications what the register which assigns the address of said storage means to the address space of said system bus is made to correspond to this storage means, and more than one are prepared in said means of communications for — the industrial computer by which it is characterized.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is used for appliance control and relates to a suitable industrial computer.
[0002]
[Description of the Prior Art] The industrial computer used for control of a device etc. has two or more I / O boards so that two or more devices can be controlled simultaneously. These I / O boards possess CPU (local CPU) to each, and this local CPU is controlling the external instrument directly. Moreover, it connects with the Maine CPU (central processing unit) board through system buses, such as a VME bus, and each I / O board shines, the control action is supervised by Maine CPU carried in the Maine CPU board, and each local CPU is controlled by it.
[0003] Moreover, by such industrial computer, the Maine CPU board has prepared CSR (control status register) used for the monitor of a I / O board in a part of VME bus address space which a VME bus manages. While this CSR is constituted by two or more registers corresponding to each application, it is made to correspond to each I / O board, and plurality is prepared. Moreover, a base address register is in one of such the CSR. This base address register is a register indicating the address of the memory which memorized the operating state of a I / O board. A mutually different value is set up so that the address set as a base address register can access the operating state of each I / O board into the VME bus address space which the Maine CPU board mentioned above, and it may not overlap between [each] I / O boards. And Maine CPU minds this base address register, and is supervising and controlling the operating state of each I / O board.
[0004]
[Problem(s) to be Solved by the Invention] By the way, LSI of high accumulation is supplied as LSI for CPU in recent years. By such LSI for CPU, circumference circuits of the conventional LSI for CPU, such as a memory circuit or an interruption circuit, are incorporated inside LSI. That is, such LSI for CPU is integrated highly for the purpose of the cutback of cost reduction and a component-side product etc. Therefore, when the I / O board mentioned above using such LSI for CPU is constituted, it is possible to attain reduction of the cost of this board and cutback-ization of board size.
[0005] However, since the capacity of the memory prepared in the interior of such LSI for CPU in this case is comparatively small, no data which must be memorized in a I / O board are memorizable to the internal memory of LSI for CPU. That is, it is necessary to prepare the external memory circuit according to individual in a I / O board in this case.
[0006] Furthermore, since the memory space of an external memory circuit was set up somewhat freely when it does in this way and two memory circuits called the internal memory and external memory circuit of LSI for CPU exist, triggered by the complicatedness which uses these separate memory circuits properly, after all, the internal memory of LSI for CPU is not used, but was operating the I / O board only using the external memory circuit. Therefore, the internal memory of LSI for CPU had the problem of becoming useless, without being used effectively. Moreover, the memory space of the part which does not use the internal memory of LSI for CPU in this case, and an external memory circuit needed to be increased, and there was a problem of becoming a cost rise.
[0007] This invention was made in view of the trouble mentioned above, and aims at offering the industrial computer which can use the internal memory of IC for CPU effectively.
[0008]
[Means for Solving the Problem] The I / O board controlled based on the control data which has two or more storage means and 1st means of communications which memorize their performance information, and is inputted into this means of communications through a system bus in order that this invention may attain the object mentioned above, It has said 1st means of communications and the 2nd means of communications which communicates through said system bus. In the industrial computer possessing the main board which reads the performance information memorized by said storage means, and supervises and controls actuation of said I / O board by this 2nd means of communications It considers as the preparing [make the register which assigns the address of said storage means to the address space of said system bus correspond to this storage means, and]-in said means of communications-more than one description.
[0009]
[Function] According to this invention, each address of the established storage means is assigned to the address space of a system bus with the register corresponding to this storage means.
[0010]
[Example] Hereafter, one example of this invention is explained with reference to a drawing. Drawing 2 is the outline block diagram of the industrial computer which is in this example. The industrial computer A is constituted by a body A-1, Maine CPU boarda, and I / O boards b0-b6 of seven sheets, and two or more connectors (graphic display abbreviation) which connect each I / O boards b0-b6 with an external instrument are prepared in the tooth back of a body A-1 so that it may illustrate.
[0011] These Maine CPU board a and each I / O boards b0-b6 are formed in the card substrate format which can be taken out and inserted freely to the body A-1, and, on the other hand, the slot corresponding to each [these] board is prepared in the body A-1, respectively. Moreover, slot number"#0" is set to the slot in which the slot number is beforehand assigned to each slot, for example, I / O board b0 is inserted. Moreover, slot number #1-#6 are set to each slot in which I / O boards b1-b6 are inserted below one by one, respectively.
[0012] Moreover, the RUN lamp c0 in which it is shown that this board is operating normally, the FAIL lamp d0 in which it is shown that it is in an unusual condition, and 7 segment LED(light emitting diode) e0 which display an abnormal condition by the

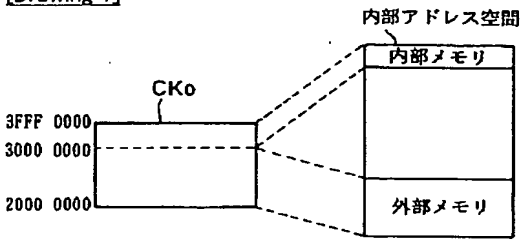
numeric value still more finely are prepared in I / O board b0, and other I / O boards b1-b6 are constituted similarly.
[0013] Next, drawing 3 is the block diagram showing the connection condition of each board mentioned above. Maine CPU board a and each I / O boards b0-b6 are connected through VME bus 1, respectively. This VME bus 1 is the system bus of the international standards used by industrial computer etc. Maine CPU board a is constituted by Maine CPUa1, ROMa2 (read-only memory), and RAMa3 (read-out / write-in memory) and the VME bus controller a4. Maine CPUa1 operates according to the program memorized by ROMa2, and carries out supervisory control of the actuation of each I / O boards b0-b6 through the VME bus controller a4. RAMa3 sets up various flags, in case Maine CPUa1 performs a program, or it memorizes operation data.
[0014] I / O board b0 is constituted by local CPUb01, ROMb02 and RAMb03, and the VME bus controller b04. Local CPUb01 communicates with Maine CPU board a through the VME bus controller b04. That is, I / O board b0 transmits and receives control information, and is supervised and controlled by Maine CPU board a by communicating with the VME bus controller a4 of Maine CPU board a through VME bus 1 by the VME bus controller b04. Local CPUb01 is memorized to the specific address in RAMb03 by making into control action information the various data delivered and received between devices 0 at this time while it controls a device 0 based on the control data which is transmitted from Maine CPU boarda and memorized by RAMb03. In addition, it is constituted completely identically [each of other I / O boards b1-b6] to I / O board b0.
[0015] Moreover, drawing 4 is the block diagram showing internal connection of I / O board b0. In this drawing, the internal bus (local bus) with which the exterior RAM where the interior RAM and b06 where it had the sign b05 in local CPUb01 was formed according to the individual in I / O board b0, and b07 connect local CPUb01, the exterior RAMb06, and VME bus controller b04 grade mutually, and b08 and b09 are mapping registers which map each address of the interior RAMb05 and the exterior RAMb06 in a VME bus address space.
[0016] The control action information to which the interior RAMb05 and the exterior RAMb06 are respectively set, for example, the internal address corresponding to an internal bus b07 mentioned them above is memorized. Local CPUb01 reads the data from the writing and the outside RAMb06 of data to the exterior RAMb06 through an internal bus b07 based on the internal address while reading the data from the writing and the interior RAMb05 of data of the interior RAMb05 based on this internal address.
[0017] On the other hand, the mapping registers b08 and b09 prepared in the VME bus controller b04 are mapped in the VME bus address space where VME bus 1 manages these interior address. That is, the VME address on the VME bus address space corresponding to the interior RAMb05 and the exterior RAMb06 is memorized by these mapping registers b08 and b09. Maine CPU board a reads the control action information memorized to the interior RAMb05 and the exterior RAMb06 by accessing the VME address memorized by these mapping registers b08 and b09, respectively. In addition, RAMb03 mentioned above is constituted by the memory which it had in the interior RAMb05, the exterior RAMb06, and the VME bus controller b04.
[0018] Next, drawing 5 is an address map in which the configuration of CSR space is shown. It consists of specifications of a VME bus so that CSR space for the Maine CPU board to supervise and control a I / O board may be established in a predetermined address space (A24 space). This CSR space is prepared so that a maximum of 21 pieces can be controlled by capacity of 512 K bytes and it can control the I / O board of 21 sheets at the maximum respectively. Now, in this example, the computer is constituted by I / O boards b0-b6 of a total of seven sheets, and the CSR space corresponding to each I / O boards b0-b6 is made to correspond to slot number #0-#6 of the body A-1 mentioned above, and turns into the CSR space CSR0-CSR6.
[0019] Next, drawing 6 is an address map in which the detail of CSR space is shown. For example, a control register R01, a status register R02, 7 segment register R03, the ID register R04, the correction register R05, and the base address register R06 are formed in the CSR space CSR 0 corresponding to I / O board b0, respectively. Each [these] register is mapped by the address respectively illustrated by the capacity of 2 bytes.
[0020] Moreover, each [these] register is prepared in the memory in the VME bus controller b04, and Maine CPU board a supervises and controls actuation of I / O board b by accessing each [these] register. In addition, each register mentioned above is mapped respectively similarly by each CSR area CSR1-CSR6 which was made to correspond to each of other I / O boards b1-b6 (slot number corresponding to these I / O boards b1-b6), and was prepared.
[0021] The control register R01 is mapped by 2 bytes of address FFFC-FFFE (hexadecimal display), and is a register which writes in the control data with which Maine CPU board a directs initialization (reset) or the self-test of I / O board b0. Local CPUb01 processes initialization or a self-test based on the control data with which Maine CPU board a was written in the control register R01.
[0022] The status register R02 is mapped by the address FFF8 - FFFA, and is a register which writes in the control data with which Maine CPU board a directs the display of a self-test result to I / O board b0. local CPUb01 -- a status register R02 -- oneself -- when the control data which directs the display of a diagnostic result is written in, when it is judged as abnormalities as a result of a diagnosis, the FAIL lamp d0 is made to turn on, and the RUN lamp c0 is made to turn on at the time of the usual actuation (normal actuation)
[0023] 7 segment register R03 is mapped by the addresses FFF4-FFF6, and is a register which writes in the control data with which Maine CPU board a directs the display of the content of the self-test result to I / O board b0. local CPUb01 -- 7 segment register R03 -- oneself -- if the control data which directs the display of the content of the diagnostic result is written in, a figure will be displayed on seven segment LEDe0 corresponding to the content of the abnormalities.
[0024] The ID register R04 is mapped by the addresses FFF0-FFF2, and is a register which tells Maine CPU board a about the ID number of I / O board b0. Local CPUb01 will output the ID number set as oneself to Maine CPU board a, if reading appearance of the ID register R04 is carried out.
[0025] The revised register R05 is mapped by address FFEC-FFEE, and is a read-out register which tells Maine CPU board a about the revised information on I / O board b0. Local CPUb01 will output the revised information on I / O board b0 to Maine CPU board a, if reading appearance of the revised register R05 is carried out.
[0026] The base address register R06 is mapped by the address FFE8 - FFEA, and the VME address at the time of mapping the internal address of the interior RAMb05 where the control action information mentioned above was memorized, and the exterior RAMb06 on a VME bus address space is memorized. That is, the internal address of the interior RAMb05 and the exterior RAMb06 is mapped by the VME address set as the base address register R06. Here, the field where control action information is mapped on this VME bus address space is called communication field. Maine CPU board a judges the operating state of I / O board b0 by accessing the communication field to which the address of this base address register R06 points.
[0027] Drawing 7 is an address map in which a VME bus address space is shown. In this drawing, Sign M is main memory by which the address of ROMa2 and RAMa3 of Maine CPU board a is mapped. Moreover, signs CK0-CK6 are communication fields,

and based on each VME address set as the base address registers R06–R66 of each I / O boards b0–b6, they are mapped so that the internal address corresponding to control action information may not overlap mutually in each I / O boards b0–b6.
[0028] Next, in the industrial computer mentioned above, if a power source is switched on and Maine CPU board a starts, Maine CPUa1 will initialize each I / O boards b0–b6 first according to the program memorized by ROMa2. namely, every in each I / O board b0 – b6 — the content of storage of RAMb03–b63 is reset. And the communication fields CK0–CK6 corresponding to each I / O boards b0–b6 are mapped as follows in the VME bus address space shown in drawing 7 .
[0029] First, Maine CPUa1 checks the capacity of main memory M, and maps the field which the main memory M concerned in a VME bus address space occupies in VME address 0000 0000–1FFF 0000. By mapping main memory M to this VME address, the intact address in a VME bus address space serves as VME address 1FFF 0001 – FFFF FFFF. Then, it directs to map Maine CPUa1 in VME address 2000 0000–3FFF 0000 memorized by the base address register R06 which mentioned above the communication field CK 0 of I / O board b0 applicable to slot number #0 for the VME bus controller b04.
[0030] At this time, the VME bus controller b04 As shown in drawing 1 , the internal address with which control action information is memorized in the exterior RAMb06 is mapped in VME address 2000 0000–3000 0000 memorized by the mapping register b08. Moreover, the internal address with which control action information is memorized in the interior RAMb05 is mapped in VME address 3000 0001–3FFF 0000 memorized by the mapping register b08. Consequently, the control action information memorized to the control action information memorized to the interior RAMb05 and the exterior RAMb06 is mapped by the address space where the communication field CK 0 continued.
[0031] henceforth — the same — carrying out — each — it is mapped by the address which the communication fields CK1–CK6 corresponding to each I / O boards b1–b6 with which slot number #1–#6 were equipped illustrate, respectively.
[0032]
[Effect of the Invention] Since each address of the established storage means is assigned to the address space of a system bus with the register corresponding to this storage means according to the industrial computer of this invention as explained above, a main board can read the information memorized by each storage means. That is, it is possible to use all the storage means established in the I / O board, and it is possible to utilize effectively the storage means in a I / O board therefore. [two or more]

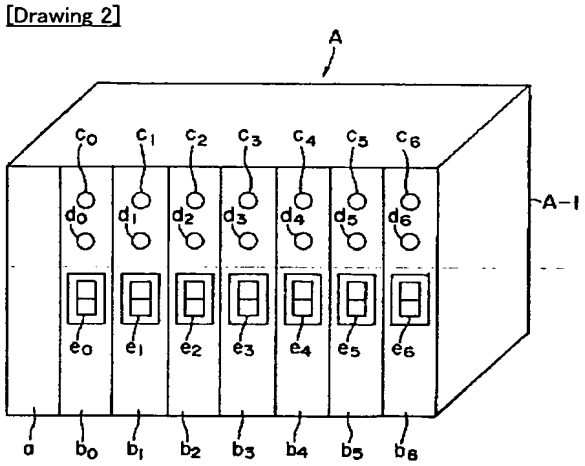
[Translation done.]

DRAWINGS

[Drawing 1]



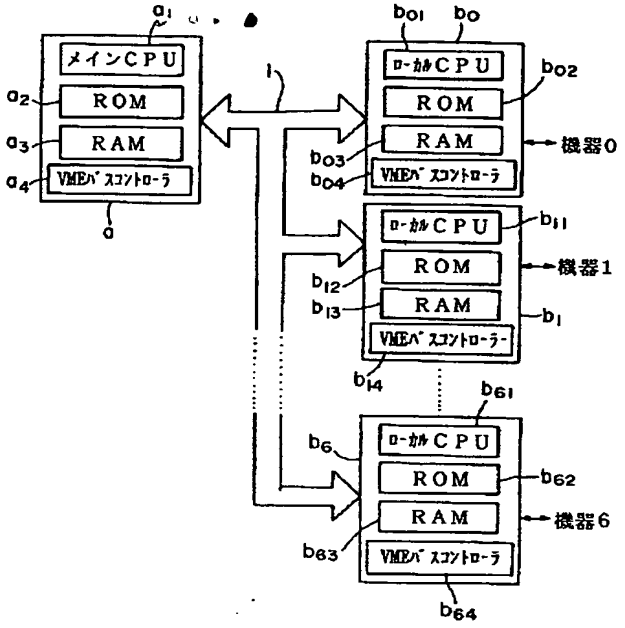
[Drawing 2]



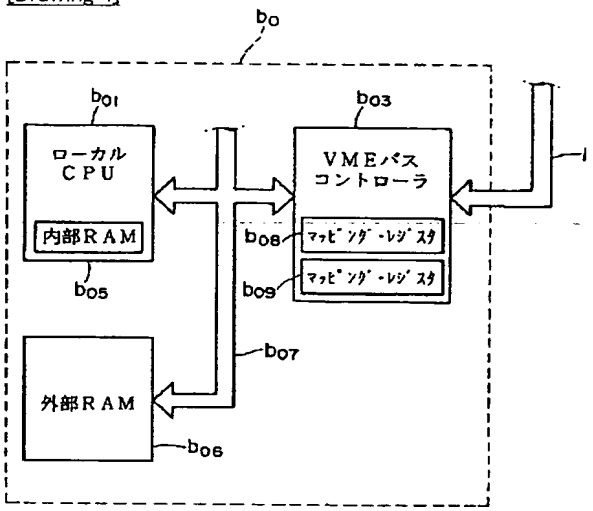
[Drawing 5]

VME #6 (512KB)	CSR6
VME #5 (512KB)	CSR5
VME #4 (512KB)	CSR4
VME #3 (512KB)	CSR3
VME #2 (512KB)	CSR2
VME #1 (512KB)	CSR1
VME #0 (512KB)	CSR0

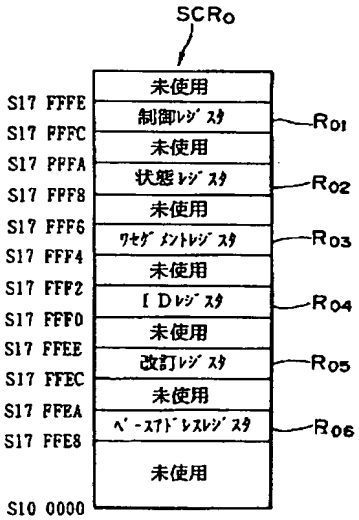
[Drawing 3]



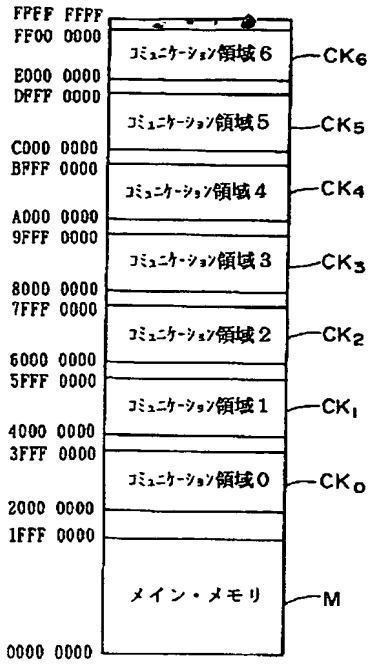
[Drawing 4]



[Drawing 6]



[Drawing 7]



[Translation done.]